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Title: ELECTRONIC ASSEMBLY COMPRISING SOLDERABLE THERMAL INTERFACE AND METHODS OF MANUFACTURE

Assignee: Intel Corporation

IN THE SPECIFICATION

Please make the paragraph substitutions indicated below. The specific changes incorporated in the substitute paragraphs are shown in the following marked-up versions of the original paragraphs.

The two paragraphs beginning on page 6, line 16 are amended as follows:

In FIG. 2, die 50 comprises a plurality of signal conductors (not shown) that terminate in pads on the <u>front or</u> bottom surface of die 50 (not shown). These pads can be coupled to corresponding lands 68 representing signal, power, or ground nodes on OLGA substrate 54 by appropriate connections such as C4 solder bumps 66. A suitable underfill 62, such as an epoxy material, can be used to surround C4 solder bumps 66 to provide mechanical stability and strength.

Still referring to FIG. 2, lid or IHS 52 forms a cover over die 50. IHS 52 is thermally coupled to a back or upper surface of die 50 through a suitable solderable thermal interface 60. In FIG. 2 the front and back surfaces of die 50 are co-planar. Die 50 can thus dissipate a substantial amount of heat through thermal interface 60 to IHS 52. The solderable thermal interface 60 comprises a material that is capable of conducting heat at a relatively high rate, and that has a relatively low melting point to minimize thermal stresses in the package when it is subjected to heat, for example during solder reflow.